39. The transistor of claim 36, wherein the insulator is formed of silicon dioxide.

40. A transistor comprising:

a source region, a drain region, a channel region between the source and drain regions, and an electrically isolated floating gate separated from the channel region by an insulator, the floating gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the gate and the insulator: and

a control gate, separated from the floating gate by an intergate dielectric.

41. The transistor of claim 40, wherein the intergate dielectric is formed of silicon dioxide.

42. The transistor of claim 40, wherein the predetermined value x is selected to provide a desired charge retention time of the floating gate.

43. The transistor of claim 40, wherein the predetermined value x is selected to provide a desired range of photon wavelengths most likely to be absorbed by the floating gate whereby electrons are emitted from the floating gate in response to the absorbed photons.

44. The transistor of claim 43, wherein the emission of electrons from the floating gate in response to incident photons changes a current conductance between the source and drain regions.

45. The transistor of claim 36, wherein the gate is formed of a material selected from the group consisting of monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

46. A device for detecting light, the device comprising:

a source region;

a drain region;

a channel region between the source and drain regions; and

a floating gate separated from the channel region by an insulator, the floating gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the floating gate and the insulator for charge storage upon the floating gate and emission of charge from the floating gate in response to absorbed incident photons.

47. The device of claim 46, further comprising a control gate located adjacent to the floating gate and separated therefrom by an interlayer dielectric.

48. The device of claim 46, wherein x is selected at a predetermined value that is approximately between 0.5 and 1.0.

49. The device of claim 46, wherein x is selected at a predetermined value to provide a desired value of the barrier energy that is approximately between 0 eV and 2.8 eV.

50. The device of claim 46, wherein the predetermined value x is selected to provide a desired range of photon wavelengths most likely to be absorbed by the floating gate whereby electrons are emitted from the floating gate in response to the absorbed photons.

51. The device of claim 46, wherein the emission of charge from the floating gate in response to incident photons changes a current conductance between the source and drain regions.

52. A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, the

floating gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the gate and the insulator; and

a control gate located adjacent to the floating gate and separated therefrom by an interlayer dielectric.

53. The device of claim 52, wherein the value of x is selected approximately between 0.5 and 1.0.

54. The device of claim 52, wherein the value of the barrier energy is approximately between 0 eV and 2.8 eV.

55. The device of claim 52, wherein the value of x is selected to provide a desired charge retention time of the floating gate.

56. A transistor comprising:

a source region formed in a silicon substrate;

a drain region formed in the silicon substrate;

a channel region in the silicon substrate between the source region and the drain region; and

a gate separated from the channel region by an insulator, the gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0 and 1.0.

57. The transistor of claim 56 wherein:

the silicon substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the silicon substrate;

the drain region comprises an n+-type drain region formed in the silicon substrate; and

the insulator comprises a layer of silicon dioxide.

58. The transistor of claim 56 wherein the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

59. A transistor comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region; and

a gate separated from the channel region by an insulator, the gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.5 and 1.0.

60. The transistor of claim 59 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate; and

the insulator comprises a layer of silicon dioxide.

61. The transistor of claim 59 wherein the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

62. A transistor comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region; and

a gate separated from the channel region by an insulator, the gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.1 and 0.5.

63. The transistor of claim 62 wherein:
the substrate comprises a p-type silicon substrate;
the source region comprises an n+-type source region formed in the substrate;
the drain region comprises an n+-type drain region formed in the substrate; and
the insulator comprises a layer of silicon dioxide.

64. The transistor of claim 62 wherein the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

65. A transistor comprising:
a source region formed in a substrate;
a drain region formed in the substrate;
a channel region in the substrate between the source region and the drain region; and
a gate separated from the channel region by an insulator, the gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be less than 0.5.

66. The transistor of claim 65 wherein:
the substrate comprises a p-type silicon substrate;
the source region comprises an n+-type source region formed in the substrate;
the drain region comprises an n+-type drain region formed in the substrate; and
the insulator comprises a layer of silicon dioxide.

67. The transistor of claim 65 wherein the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

68. A floating gate transistor comprising:

a source region formed in a silicon substrate;

a drain region formed in the silicon substrate;

a channel region in the silicon substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0 and 1.0; and

a control gate separated from the floating gate by an intergate dielectric.

69. The floating gate transistor of claim 68 wherein:

the silicon substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the silicon substrate;

the drain region comprises an n+-type drain region formed in the silicon substrate;

the insulator comprises silicon dioxide; and

the intergate dielectric comprises silicon dioxide.

70. The floating gate transistor of claim 68 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

71. A floating gate transistor comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.5 and 1.0; and

a control gate separated from the floating gate by an intergate dielectric.

72. The floating gate transistor of claim 71 wherein:
the substrate comprises a p-type silicon substrate;
the source region comprises an n+-type source region formed in the substrate;
the drain region comprises an n+-type drain region formed in the substrate;
the insulator comprises silicon dioxide; and
the intergate dielectric comprises silicon dioxide.

73. The floating gate transistor of claim 71 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

74. A floating gate transistor comprising:
a source region formed in a substrate;
a drain region formed in the substrate;
a channel region in the substrate between the source region and the drain region;
a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.1 and 0.5; and
a control gate separated from the floating gate by an intergate dielectric.

75. The floating gate transistor of claim 74 wherein:
the substrate comprises a p-type silicon substrate;
the source region comprises an n+-type source region formed in the substrate;
the drain region comprises an n+-type drain region formed in the substrate;
the insulator comprises silicon dioxide; and
the intergate dielectric comprises silicon dioxide.

76. The floating gate transistor of claim 74 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a

polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

77. A floating gate transistor comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be to be less than 0.5; and

a control gate separated from the floating gate by an intergate dielectric.

78. The floating gate transistor of claim 77 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate;

the insulator comprises silicon dioxide; and

the intergate dielectric comprises silicon dioxide.

79. The floating gate transistor of claim 77 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

80. A floating gate transistor comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.5 and 0.75; and

a control gate separated from the floating gate by an intergate dielectric.

81. The floating gate transistor of claim 80 wherein:
the substrate comprises a p-type silicon substrate;
the source region comprises an n+-type source region formed in the substrate;
the drain region comprises an n+-type drain region formed in the substrate;
the insulator comprises silicon dioxide; and
the intergate dielectric comprises silicon dioxide.

82. The floating gate transistor of claim 80 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

83. A floating gate transistor comprising:
a source region formed in a substrate;
a drain region formed in the substrate;
a channel region in the substrate between the source region and the drain region;
a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.75 and 1.0; and
a control gate separated from the floating gate by an intergate dielectric.

84. The floating gate transistor of claim 83 wherein:
the substrate comprises a p-type silicon substrate;
the source region comprises an n+-type source region formed in the substrate;
the drain region comprises an n+-type drain region formed in the substrate;
the insulator comprises silicon dioxide; and
the intergate dielectric comprises silicon dioxide.

85. The floating gate transistor of claim 83 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

86. A system comprising:

a processor; and

a memory device coupled to the processor through a plurality of lines, the memory device comprising:

a control circuit; and

an array of floating gate transistor memory cells, each memory cell comprising:

a source region formed in a silicon substrate;

a drain region formed in the silicon substrate;

a channel region in the silicon substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0 and 1.0; and

a control gate separated from the floating gate by an intergate dielectric.

87. The system of claim 86 wherein:

the silicon substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the silicon substrate;

the drain region comprises an n+-type drain region formed in the silicon substrate;

the insulator comprises silicon dioxide;

the intergate dielectric comprises silicon dioxide;

the lines comprise control lines, data lines, and address lines; and

the memory device further comprises a row decoder, a column decoder, and a voltage control circuit.

88. The system of claim 86 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

89. A system comprising:

a processor; and

a memory device coupled to the processor through a plurality of lines, the memory device comprising:

a control circuit; and

an array of floating gate transistor memory cells, each memory cell comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.5 and 1.0; and

a control gate separated from the floating gate by an intergate dielectric.

90. The system of claim 89 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate;

the insulator comprises silicon dioxide;

the intergate dielectric comprises silicon dioxide;

the lines comprise control lines, data lines, and address lines; and

the memory device further comprises a row decoder, a column decoder, and a voltage control circuit.

91. The system of claim 89 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

92. A system comprising:

a processor; and

a memory device coupled to the processor through a plurality of lines, the memory device comprising:

a control circuit; and

an array of floating gate transistor memory cells, each memory cell comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.5 and 0.75; and

a control gate separated from the floating gate by an intergate dielectric.

93. The system of claim 92 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate;

the insulator comprises silicon dioxide;

the intergate dielectric comprises silicon dioxide;

the lines comprise control lines, data lines, and address lines; and

the memory device further comprises a row decoder, a column decoder, and a voltage control circuit.

94. The system of claim 92 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

95. A system comprising:

a processor; and

a memory device coupled to the processor through a plurality of lines, the memory device comprising:

a control circuit; and

an array of floating gate transistor memory cells, each memory cell comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.75 and 1.0; and

a control gate separated from the floating gate by an intergate dielectric.

96. The system of claim 95 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate;

the insulator comprises silicon dioxide;

the intergate dielectric comprises silicon dioxide;

the lines comprise control lines, data lines, and address lines; and

the memory device further comprises a row decoder, a column decoder, and a voltage control circuit.

97. The system of claim 95 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

98. The transistor of claim 36, wherein the gate is an electrically isolated floating gate and further comprising a control gate, separated from the floating gate by an intergate dielectric comprising silicon dioxide.

99. The transistor of claim 37 wherein:

the insulator comprises silicon dioxide; and

the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

100. The transistor of claim 40 wherein:

the insulator comprises silicon dioxide; and

the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

REMARKS

The original claims 1-35 have been canceled without prejudice, and new claims 36-100 have been added.

The applicant notes that U.S. Patent No. 5,801,401 to Forbes has been used as a reference in support of rejection under 35 U.S.C. § 103(a) in the parent U.S. Application Serial No. 08/903,452, filed on July 29, 1997, and from which priority is claimed. Forbes issued on September 1, 1998, which is after the July 29, 1997 filing date of the prior U.S. Application Serial Number 08/903,452, which is relied upon for an earlier filing date under 35 U.S.C. §120, as is listed above in the amendment to the specification. The Examiner therefore applied Forbes as prior art only under 35 U.S.C. § 102(e). The applicant does not admit that Forbes is prior art